A reconfigurable active quenching system : Towards automated characterization of custom chip-scale APDs

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MOTIVATION

Most active quench circuits used for single-photon avalanche detectors are designed either with only discrete components [1] which lack the flexibility of dynamically changing the control parameters, or with custom ASICs [2] which require a long development time and high cost. As an alternative, we present a reconfigurable hybrid design implemented using very few discrete parts and a System-on-Chip (SoC), which integrates both an FPGA and a microcontroller. This paves way for automated wafer-scale testing and characterization of large number of custom fabricated integrated APDs without the need for additional packaging and interconnects.

DESIGN FEATURES AND OPERATION

- FPGA allows to change Quench and Reset durations instantly
- Microcontroller interfaces with PC to enable remote configuration of FPGA and automated characterization of APD
- FPGA/SoC can be placed far from APD head (as far as 15cm)
- Suitable for applications such as telecommunications and quantum key distribution (QKD)

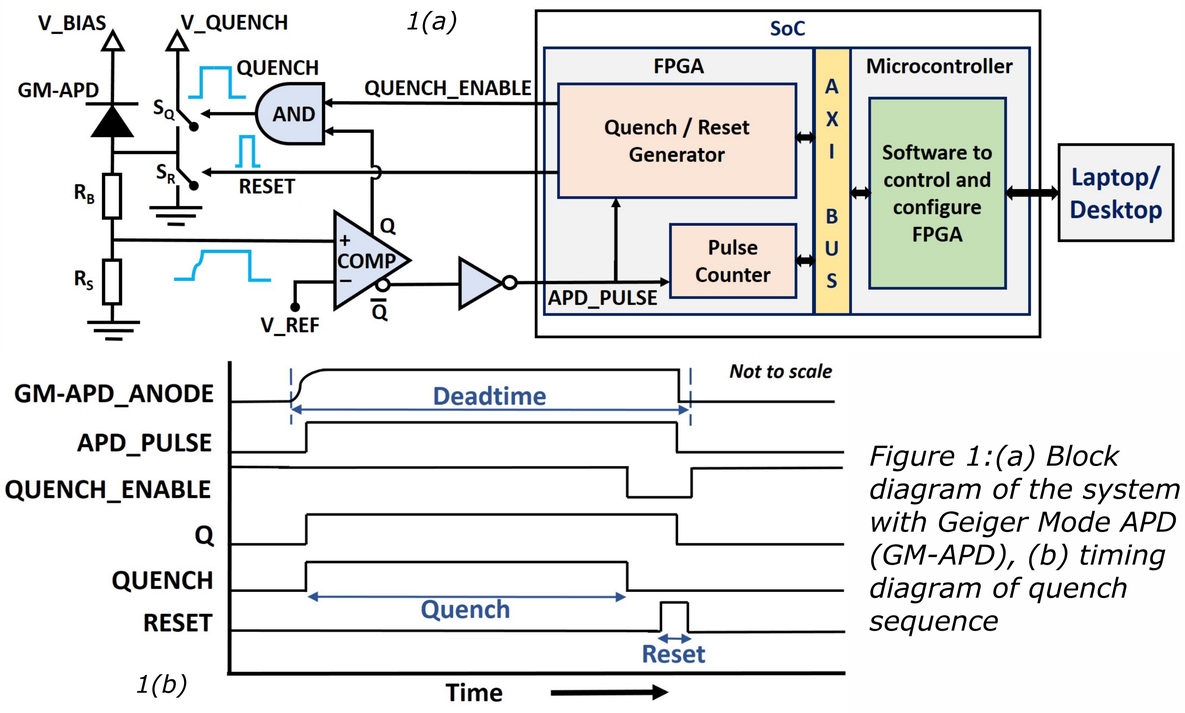


Figure 1:(a) Block diagram of the system with Geiger Mode APD (GM-APD), (b) timing diagram of quench sequence

PERFORMANCE AND FLEXIBILITY

RECONFIGURABLE PARAMETERS			
	Min.	Max.	Units
Quench duration	20	1000	ns
Reset duration	5	1000	ns
Deadtime	35	1000	ns
Quench Voltage	0	30	V
Bias Voltage	0	500	V

- Hybrid implementation with a custom PCB and *Zedboard* kit [3] having a *Zynq-7000 SoC*
- Smallest deadtime of 35ns
- Pulse counting up to 16Mcps
- For a deadtime of 35ns, after-pulsing probability is ~5% with SAP500 APD cooled down to 263K
- Above performance metrics makes the setup suitable for practical QKD implementations as described in [1]

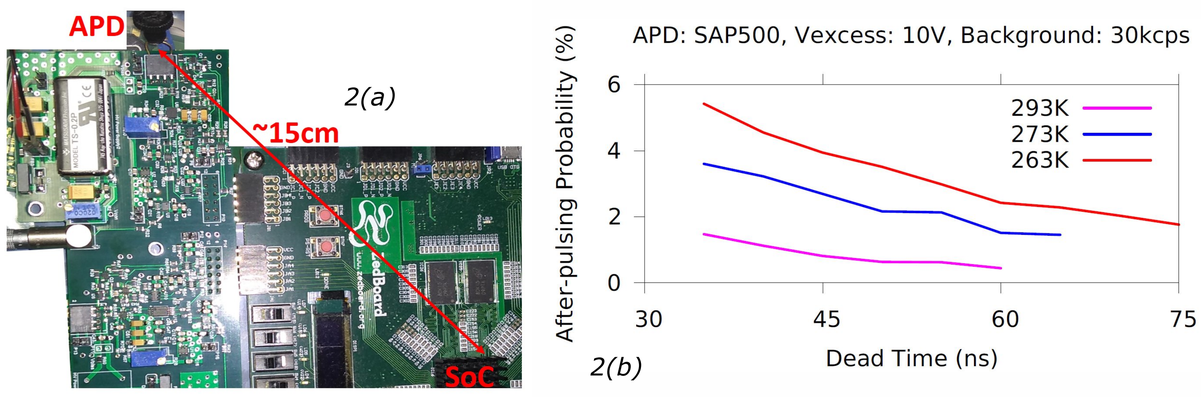
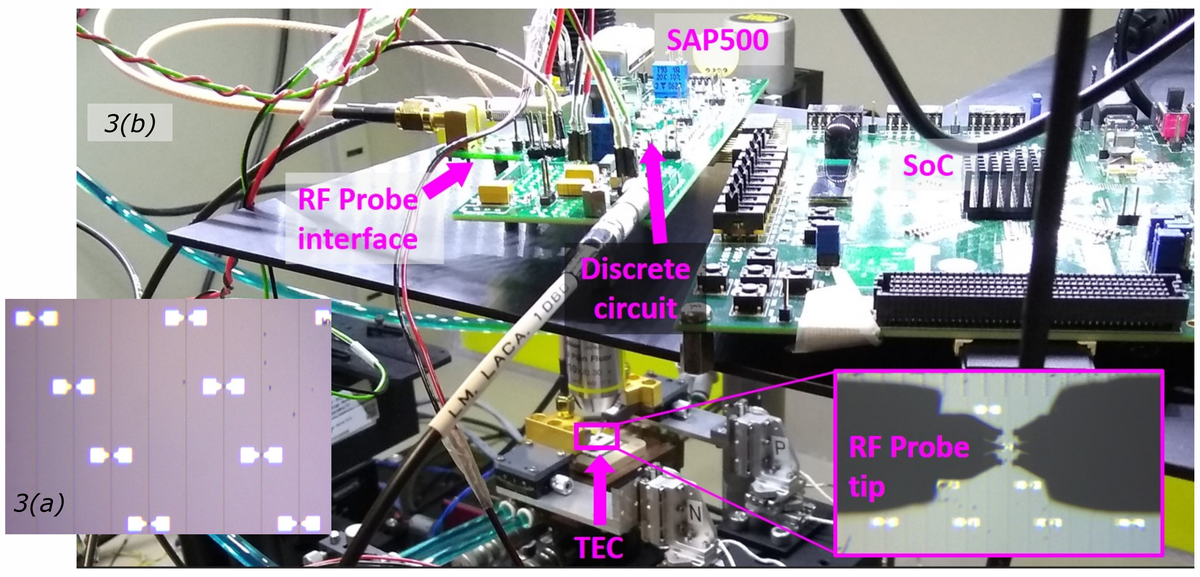


Figure 2:(a) Test setup with the SAP500 APD located 15cm away from SoC, (b) After-pulsing measurements for test setup at varying deadtime and temperatures

INTEGRATION WITH CUSTOM CHIP-SCALE APD

- Successfully tested with custom fabricated integrated APD [4] without any modification to existing active quench design
- Active quench system stops the APD breakdown voltage drift by forward biasing the APD during the quenching process
- High rate of avalanche pulses (>1Mcps) can be detected despite large separation between APD and SoC
- Next step: Optimize hardware and software of active quenching system to enable large-scale automated testing



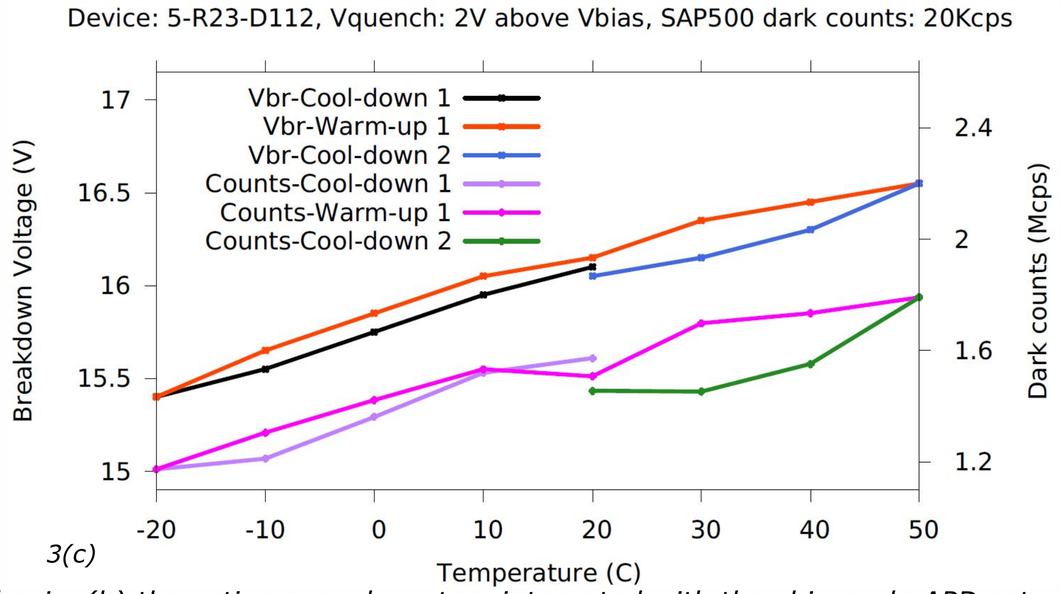


Figure 3: (a) the pads of APDs on a single chip connected with optical waveguides along vertical axis, (b) the active quench system integrated with the chip-scale APD set up. RF probes (inset) connect the APD to the custom active quench system. The APD can be cooled down to -20C by a TEC, (c) breakdown voltage and dark counts obtained for an on-chip APD at different temperatures using this setup.

REFERENCES

1. *M Stipčević, et al., Opt. Express, vol. 25, no. 18, pp. 21 861–21 876, Sep 2017*
2. *G. Acconcia, et al., Opt. Express, vol. 24, no. 16, pp. 17 819–17 831, Aug 2016*
3. *Zedboard development kit - http://zedboard.org/product/zedboard*
4. *S. Yanikgonul, et al., Nature Communications, 12, 1834, March 2021*

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