Simulation of Silicon Waveguide Single-photon Avalanche Diodes for Integrated Photonics

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Introduction

Integrated photonic platforms are promising candidates for the development and implementation of scalable quantum information and networking schemes. However, many state-of-the-art photonic platforms still require the coupling of light to external photodetectors. On-chip silicon single-photon avalanche diodes (SPAD) are a viable option as they can be fabricated at scale and can be operated near room temperature with high efficiencies [1]. We report the design and simulation of waveguide-based silicon SPADs for visible wavelengths (640 nm). For our simulated parameters, we obtained a maximum PDE of 55% at a reverse bias voltage of 34.5 V with timing jitter of ≈ 6 ps and dark count rate (DCR) of ≈ 3 sec^{-1} at 243 K.

Silicon Waveguide SPAD Design

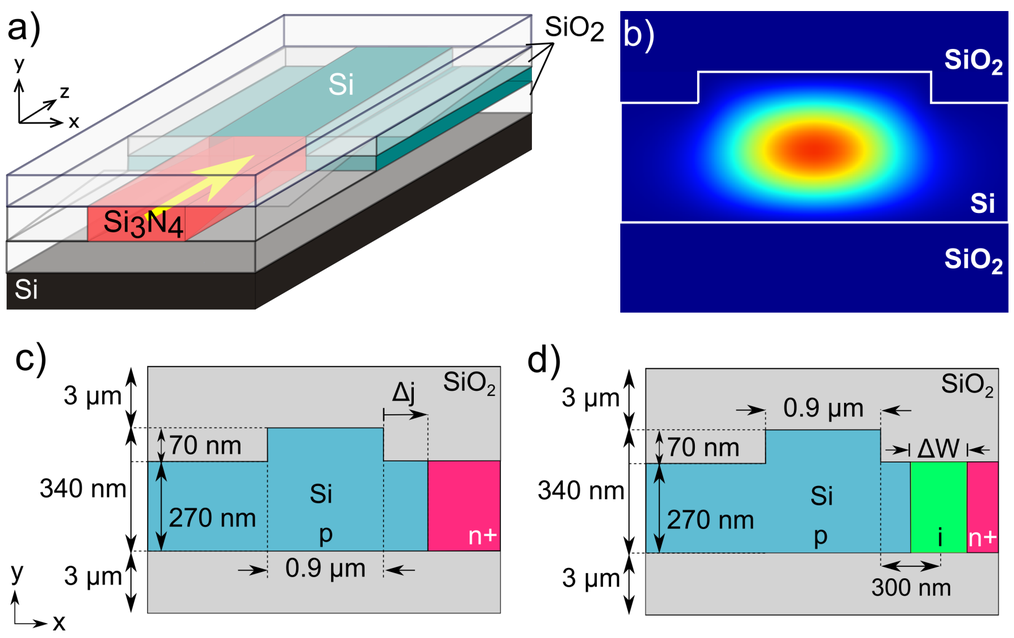

FIGURE 1: (a) SPAD structure, consisting of a Si rib waveguide end-fire coupled to an input Si_3N_4 waveguide, (b) optical mode profile at 640 nm for the fundamental (quasi-)TE mode, (c) p-n$^+$ SPAD doping profile with a junction placed different distances Δj from the right edge of the rib, (d) p-i-n$^+$ SPAD doping profile with various intrinsic region width ΔW.

Device Geometry: The SPADs are based on SOI platform, and consists of a 16 μm long silicon (Si) rib waveguide with an absorption of $> 99\%$ at 640 nm. Input light is end-fire coupled from a Si_3N_4 waveguide, which has low propagation losses at visible wavelengths. The end-fire optical coupling efficiency of the fundamental (quasi)-TE mode is $> 90\%$. We fix the waveguide width and height at 900 nm and 340 nm respectively, while the rib height of 270 nm is designed to minimize the loss of charge carriers during the avalanche process, which would have reduced the PDE.

Doping Profile: We study two device families with different doping profiles: p-n$^+$ and p-i-n$^+$. In p-n$^+$ SPADs, we study the effect of the juction position Δj, whereas we vary the intrinsic region width ΔW in p-i-n$^+$ devices.

DC Electrical Analysis

Using device dimension and doping profiles, we perform DC electrical analysis of SPADs (ATLAS, Silvaco Inc.) to obtain the electric field and the charge carrier mobilities, drift velocities, and ionization coefficients.

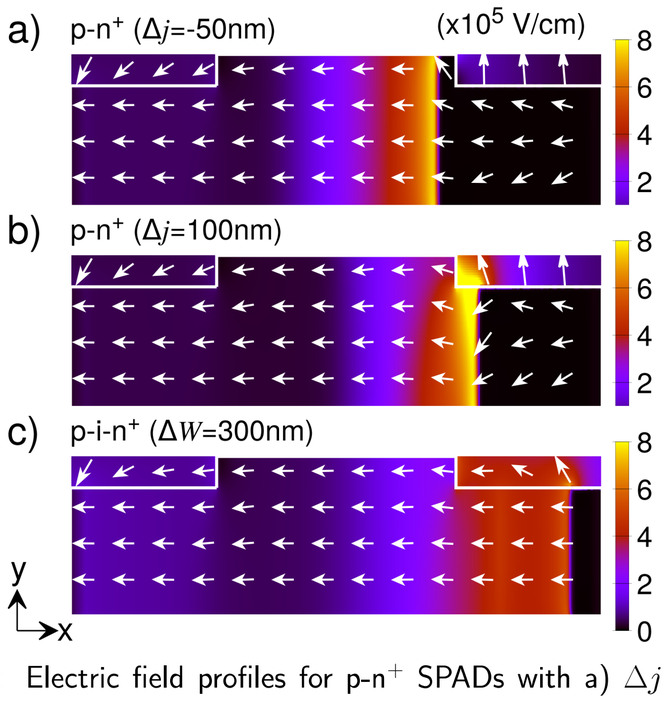

FIGURE 2: Electric field profiles for p-n$^+$ SPADs with a) $\Delta j = -50$ nm at $V_B = 21.5$ V, b) $\Delta j = 100$ nm at $V_B = 20.7$ V, and c) for p-i-n$^+$ SPAD with $\Delta W = 300$ nm at $V_B = 21.5$ V.

2D Monte Carlo Simulation and DCR calculation

We use these parameters in our Monte Carlo simulator to simulate the avalanche multiplication of charge carriers following the absorption of an input photon [2] and perform 6000 simulation runs to simulate a device for a given reverse bias voltage (V_B). A run results in a successful avalanche if the device current crosses a predefined current threshold. The PDE is defined as the fraction of runs with successful avalanches. The timing jitter is defined by the interquartile range of the distribution of avalanche detection times.

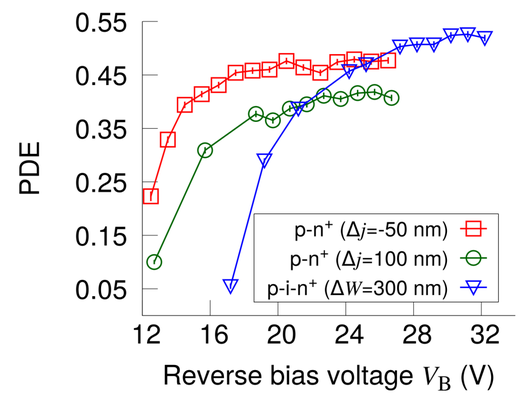

FIGURE 3: Representative curves showing PDE vs. V_B for p-n$^+$ SPADs with $\Delta j = -50$ nm and $\Delta j = 100$ nm, and for p-i-n$^+$ SPAD with $\Delta W = 300$ nm.

We study DCR at 243 K and 300 K for p-n$^+$ and p-i-n$^+$ SPADs with the highest PDEs. We consider the Shockley-Read-Hall trap assisted tunneling (TAT) process with Si/SiO_2 interface trap levels as well as band-to-band tunneling (BTBT) process for dark carrier generation.

PDE and timing jitter: In Fig. 4, we report timing jitters and saturated PDEs, which we define as the mean of the PDEs that are within the uncertainty at 3 subsequent bias voltages which are 1 V apart. In p-n$^+$ SPADs, the highest saturated PDE is obtained $48.1 \pm 0.6\%$ for a device with $\Delta j = 400$ nm with a timing jitter of around 5 ps at $V_B = 25.5$ V. In p-i-n$^+$ devices, the optimum performance parameters of PDE and timing jitter is obtained for a device with $\Delta W = 400$ nm, which has a saturated PDE of $51.9 \pm 0.6\%$ with a timing jitter of around 6 ps at $V_B = 30.5$ V.

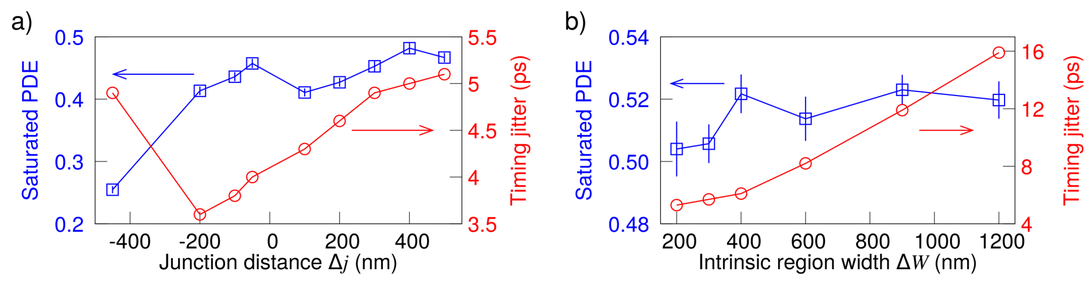

FIGURE 4: PDE and timing jitter values at a V_B where PDE saturates, (a) for p-n$^+$ SPADs with different junction distances Δj and (b) for p-i-n$^+$ SPADs with various intrinsic region widths ΔW. Error bars show s.d. uncertainty.

DCR: We calculate DCRs according to the following volume integral:

$$DCR = \int L \cdot P_{\text{trig}}(\mathbf{r}) \cdot (G_{\text{TAT}}(\mathbf{r}) + G_{\text{BTBT}}(\mathbf{r}))\ \mathrm{d}\mathbf{r}$$

where L is the length of the device and $P_{\text{trig}}(\mathbf{r})$ is the avalanche triggering probability of a charge carrier with a position vector $\mathbf{r}$. $G_{\text{TAT}}(\mathbf{r})$ and $G_{\text{BTBT}}(\mathbf{r})$ are the generation rates per unit volume (cm^{-3} · sec^{-1}) due to TAT and BTBT processes, respectively.

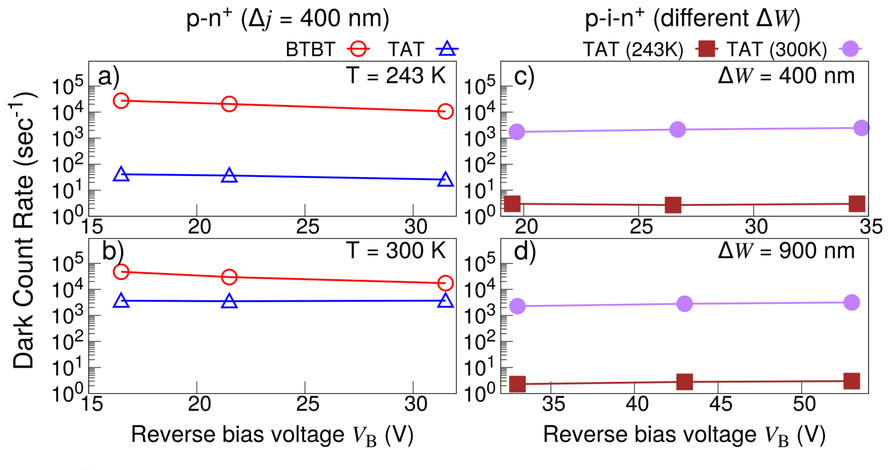

FIGURE 5: DCR vs. V_B for p-n$^+$ SPAD with $\Delta j = 400$ nm at a) 243 K and b) 300 K, and for p-i-n$^+$ SPAD with c) $\Delta W = 400$ nm and d) $\Delta W = 900$ nm at 243 K and 300 K. DCR due to BTBT is negligible for p-i-n$^+$ SPADs so it is not shown here.

References:

[1] Nat. Photonics **3**, 687 - 695 (2009)
[2] Opt. Express **26**, 15232 - 15246 (2018)